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Self-aligned vertical double-gate MOSFET (VDGM) with the oblique rotating ion implantation (ORI) method

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ABSTRACT

A process of making a symmetrical self-aligned n-type vertical double-gate MOSFET (n-VDGM) over a silicon pillar is revealed. This process utilizes the technique of oblique rotating ion implantation (ORI). The self-aligned region forms a sharp vertical channel profile and decreases the channel length L_g. A tremendous improvement in the drive-on current is noted. The electron concentration profile obtained demonstrates an increased number of electrons in the channel injected from the source end as the drain voltage increases. The enhanced carrier concentration results in significant reduction in the off-state leakage current and improves the drain-induced barrier-lowering (DIBL) effect. These simulated characteristics when compared to those in a fabricated device without the ORI method show the distinct advantage of the technique reported for suppression of short-channel effects (SCE) in nanoscale vertical MOSFET.

1. Introduction

Aggressive scaling of complementary metal-oxide semiconducting (CMOS) technology to nanoscale dimensions requires an innovative approach for overcoming various physical limits. One such limit is the minimum gate oxide (t_{OX}) thickness required to limit the undesirable gate leakage. The corresponding short-channel effects (SCE) include leakage current, drain-induced barrier lowering (DIBL), threshold voltage (V_T) roll-off and velocity saturation. All these effects need to be carefully examined in assessing the performance behavior. A channel on a side of an insulating pillar made of SiO_2 in a vertical MOSFET is forecasted to be an attractive solution [1] for sustaining the scaling of CMOS technology into nanometer regime. This structure offers a number of advantages over planar MOSFET [2]. Firstly, the channel length (L_g) has no dependence on the critical lithography. Secondly, the vertical MOSFET can double the channel width per transistor area, leading to an increased packing density and the drive-on current that is twice as large. Thirdly, a fully depleted (FD) vertical MOSFET provides an almost ideal sub-threshold slope and excellent SCE immunity. Considering these advantageous features, the vertical double-gate MOSFET (VDGM) is suitable for high-density, low-voltage, and low-power DRAM applications.

In general, there are two methods to fabricate vertical MOSFET. One alternative is to utilize the epitaxial growth such as molecular beam epitaxy (MBE) [3–5]. However, this approach is not CMOS compatible. The other alternative is to etch silicon pillars and then diffuse the implanted dopants [6]. Nevertheless, the minimum channel length that can be achieved in this way is limited by the height of silicon pillar and by the thickness of nitride fillets [7]. Non-self-aligned channels also contribute to this problem. As a result, unacceptable high V_T and DIBL, large leakage current and low drive current are observed for a device with $L_g = 125$ nm. This limits the scaling of a device to nanoscale. To address these problems, an oblique rotating ion implantation (ORI) method was employed for making a self-aligned symmetrical source/drain region over the silicon pillar. In this way, a sharp vertical channel profile over a pillar is obtained, which improved the current drivability and the controllability of threshold voltage [8]. Subsequently, these desirable features are able to suppress the SCE when scaling the device into the nanometer regime [9–11].

In Section 2, the process simulation [12] leading to the device structure studied is presented. This is followed by the device simulation to obtain the I–V characteristics in Section 3. Section 4 gives the analysis of doping profiles resulting in electron concentration in the channel. Comparative outcomes are discussed in Section 5, with and without the ORI method. The major findings of this work are summarized in the concluding Section 6.

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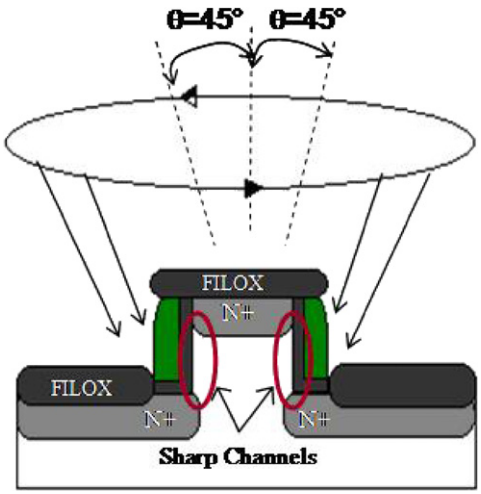

Fig. 1. Cross-section of vertical MOSFET with oblique rotating ion implantation (ORI).

2. Device structure

The proposed device structure is similar to vertical MOSFET with fillet-local-oxidation (FILOX) for parasitic capacitance reduction [13]. However, here the structure has been enhanced with a symmetrical self-aligned source/drain region and a sharp vertical channel profile over the silicon pillar. The method of ORI is employed to reveal this unique feature of the device structure. Fig. 1 shows the cross-section view of an n-VDGM fabricated using the ORI method.

Prior to the device fabrication process, a finer mesh is defined for the critical area in the vicinity of the channel. The p-type boron-doped ($1\times10^{19}\,\mathrm{cm}^{-3}$) silicon wafer $\langle 1\,0\,0\rangle$ is used as the substrate. Dry etch of the silicon pillars is carried out to a height of about 220 nm using nitride masks. Stress relief oxide of 20 nm was thermally grown using dry oxygen to relieve the stress between the ensuing nitride layer and silicon. A nitride layer is deposited that is followed by active area definition through anisotropic dry etch. Subsequently, formation of FILOX took place by thermally grown 60-nm-thick oxide layers. The area protected by the nitride spacers was not affected by oxide growth; thus a thick oxide layer was formed on the whole active area and on the top of the pillar. The self-aligned source/drain regions are implanted using 45° tilt Arsenic with a dose of $6\times10^{15}\,\mathrm{cm}^{-2}$ and energy of 150 keV. This process was repeated again after 180° wafer rotation for the other side of the pillar (Fig. 1). The stress relief oxide is removed by an isotropic wet etch leaving an approximately 40-nm-thick FILOX oxide on the top and bottom of the pillar. A 3 nm gate oxide is thermally grown on the sidewall of the pillar. Then a 200 nm in-situ n+ doped (As, $5\times10^{19}\,\mathrm{cm}^{-3}$) polysilicon layer is deposited and patterned by dry etch. In this way n-type polysilicon spacers are created on the left and right of the pillar for double-gate definition. A thick oxide isolation layer was then deposited and rapid thermal annealing (RTA) at 1100 °C for 0.17 min is performed for dopant activation. Geometrical etch of oxide is done to open a window for drain electrodes deposited and patterned. A mask is used to cover the drain electrodes from the subsequent process of opening source window, depositing aluminum and patterning source contacts.

3. Device simulation

Various electrical characteristics of devices were done by solving Poisson's equation and continuity equation numerically and self-consistently within explicitly defined meshes of the devices. The electrical potential energy and electronic band structures can be computed using Poisson's equation. Continuity equations for electrons and holes are then used to calculate the current densities of electrons and holes. The Boltzmann transport framework is used in solving these two equations. The relationship between the current density of electrons/holes and carrier concentration as well as the quasi-Fermi potential is exhibited during this self-consistent process. Since vertical MOSFET is a non-planar device, the correlation between carrier mobility, carrier concentration, temperature and the electric field can be described as a semi-empirical equation presented in Ref. [14]. In a low electric field, the carrier mobility is given by three components that are combined using Matthiessen's rule

$$\mu_{\mathrm{T}}^{-1}=\mu_{\mathrm{AC}}^{-1}+\mu_{\mathrm{b}}^{-1}+\mu_{\mathrm{sr}}^{-1} \tag{1}$$

μ_{AC} is the surface mobility limited by scattering with acoustic phonons given by

$$\mu_{\mathrm{AC}}=\frac{B}{E_{\perp}}+\frac{CN^{1/8}}{T_{\mathrm{L}}E_{\perp}} \tag{2}$$

where $B=4.75\times10^{7}\,\mathrm{cm/s}$, $C=1.74\times10^{5}$, N is the total doping concentration, $E_{\perp}$ the transverse field and T_{L} is the lattice temperature in Kelvin. μ_{b} is the mobility limited by scattering with optical intervalley phonons given by

$$\mu_{\mathrm{b}}=\mu_{0}+\frac{\left|\mu_{\mathrm{m}}(T_{\mathrm{L}}/300)^{-2.5}-\mu_{\mathrm{o}}\right|}{1+(N_{\mathrm{A}}/C_{\mathrm{r}})^{0.680}}-\frac{\mu_{1}}{1+(C_{\mathrm{s}}/N_{\mathrm{A}})^{2}} \tag{3}$$

where $\mu_{\mathrm{o}}=52.2\,\mathrm{cm}^2/(\mathrm{V\,s})$, $\mu_{\mathrm{m}}=1417\,\mathrm{cm}^2/(\mathrm{V\,s})$, $\mu_{1}=43.4\,\mathrm{cm}^2/(\mathrm{V\,s})$, $C_{\mathrm{r}}=9.86\times10^{16}\,\mathrm{cm}^{-3}$, $C_{\mathrm{s}}=3.43\times10^{20}\,\mathrm{cm}^{-3}$ and N_{A} is the total density of impurities. μ_{sr}, the surface roughness factor for electrons, is given by

$$\mu_{\mathrm{sr}}=\delta/E_{\perp}^{2} \tag{4}$$

where $\delta=5.82\times10^{14}\,\mathrm{cm}^2/(\mathrm{V\,s})$. The mobility degradation due to presence of the electric field is given by the relation

$$\mu_{n}(E_{\parallel})=\mu_{n0}[1/1+(\mu_{n0}E_{\parallel}/\mathrm{VSATN})]^{\frac{1}{2}} \tag{5}$$

where μ_{n0} is the electrons low-electric-field mobility and $E_{\parallel}$ is the longitudinal electric field in the direction of current. VSATN is the saturated drift velocity calculated from the temperature-dependent model [15]

$$\mathrm{VSATN}=v^{*}/1+C\exp(T_{\mathrm{L}}/\theta) \tag{6}$$

where $v^{*}=2.4\times10^{7}\,\mathrm{cm/s}$, $C=0.8$ and $\theta=600\,\mathrm{K}$. The recombination behaviors between electrons and holes are described by Shockley–Read–Hall equation with fixed carrier lifetimes. An interface fixed oxide charge of $3\times10^{10}\,\mathrm{C/m}^2$ is assumed with the presence of an n-type polysilicon gate.

4. Device profiles analysis

The vertical and horizontal doping profiles of the device are shown in Fig. 2. The effective channel length L_g is 50 nm as observed in Fig. 2(a). Also shown is the boron-doping profile ranging from 5×10^{18} to $7.45\times10^{18}\,\mathrm{cm}^{-3}$ in the channel. Arsenic-doping profiles for the source and the drain have a peak value of 2.60×10^{20} and $3.53\times10^{20}\,\mathrm{cm}^{-3}$, respectively. In Fig. 2(b) the silicon thickness $t_{\mathrm{si}}=136\,\mathrm{nm}$ is shown, which indicates the partially depleted (PD) operation of the device. The junction depth for the source is 106 nm, giving a sheet resistance of 33 Ω/sq. The junction depth for the drain is 126 nm, giving a sheet resistance of 16 Ω/sq. The high body doping is needed for overcoming SCE [16]. The degradation of the carrier mobility

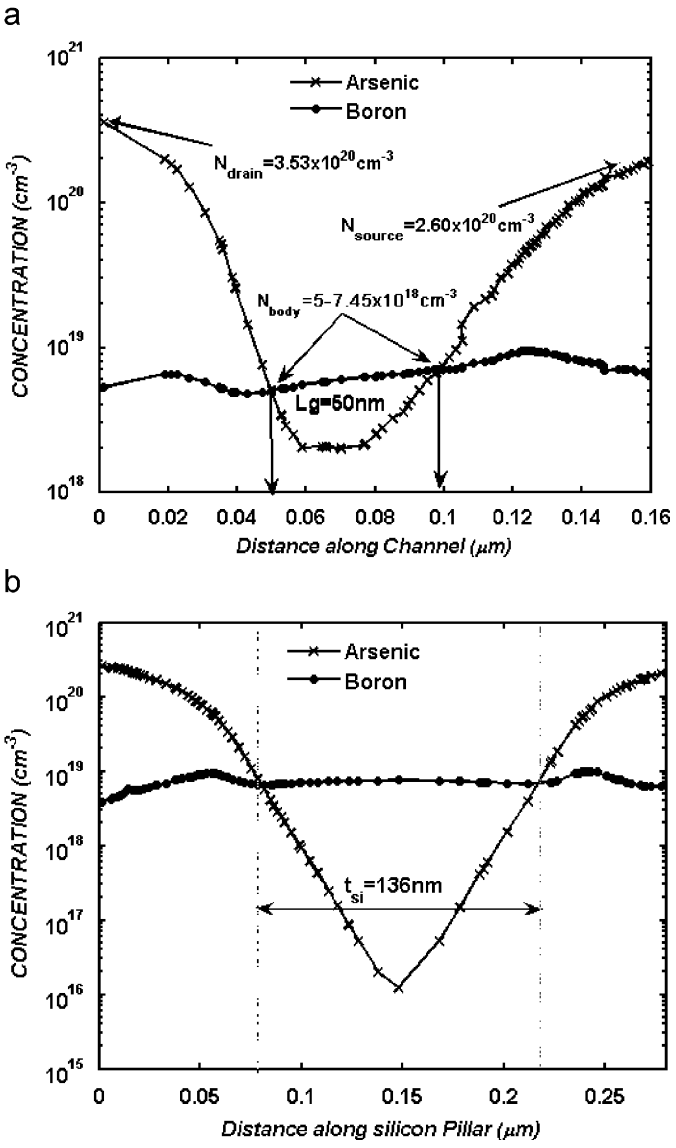

Fig. 2. Doping profile of vertical double-gate MOSFET (a) vertical doping shows region doping & $L_g = 50$ nm (b) horizontal doping shows $t_{si} = 136$ nm.

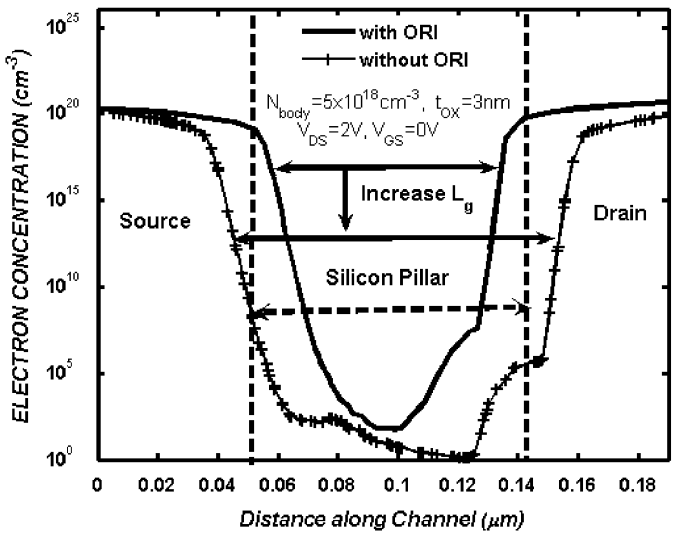

Fig. 3. Electron concentration profile of vertical double-gate MOSFET for both with and without the ORI method at $V_{DS} = 2$ V and $V_{GS} = 0$ V.

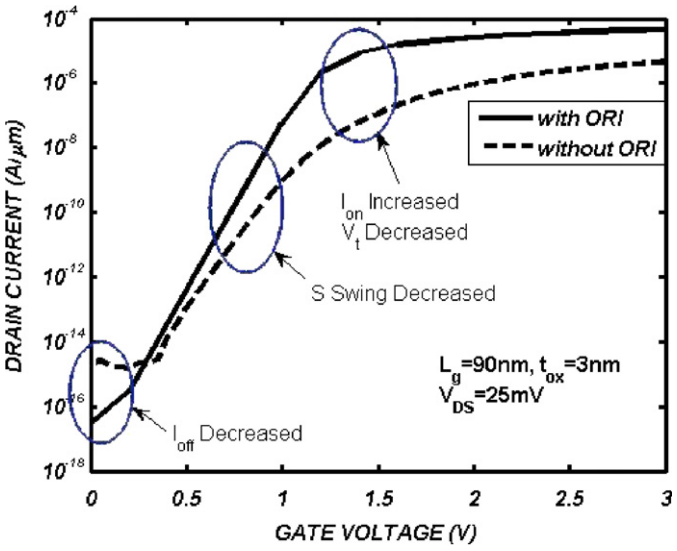

Fig. 4. Sub-threshold characteristics of vertical double-gate MOSFET for both with and without the ORI method at $V_{DS} = 25$ mV and $L_g = 90$ nm.

inside the nanoscale channel will effectively reduce the leakage current and sustain the threshold voltage roll-off. The low source and drain sheet resistance suggest that the ORI method can control the junction depth in enhancing the drive-on current.

Fig. 3 illustrates the electron concentration profile along the vertical channel from the source to the drain region approximately 2 nm below the Si–SiO_2 interface for both vertical MOSFETs fabricated with the ORI and without ORI technique at $V_{DS} = 2$ V and $V_{GS} = 0$ V. As depicted in Fig. 3, vertical MOSFET with the ORI device has a larger concentration of electrons inside the channel injected from the source as the drain voltage increases compared to that without the ORI method. This is mainly due to the symmetrical self-aligned source/drain region over the silicon pillar during the tilted and rotated ion implantation process. Therefore, the off-state leakage current and DIBL effect can be reduced significantly. In addition, the self-aligned regions create a sharp vertical channel profile over the silicon pillar and reduce the channel length. As a result, an improved drive-on current can be observed prominently.

5. Results and discussion

Fig. 4 demonstrates the comparison of sub-threshold characteristic for 90 nm VDGM in ORI and without the ORI device at $V_{DS} = 25$ mV. The off-state leakage current I_{off} due to electrons diffused into the substrate is shown to be lower by at least two decades in an ORI device. A significant decrease in sub-threshold swing and threshold voltage is visible in Fig. 2 for an ORI device. The sub-threshold swing declined from 160 to 100 mV/dec and the threshold voltage V_T from 1.2 to 0.56 V without and with the ORI method, respectively. Higher drive-on current I_{on} is observed in the ORI device, which increased by a factor of 2 as compared to that without the ORI method. The measured DIBL defined as $V_{T(Vds = 0.025V)} - V_{T(Vds = 1.0V)}$ is 94 and 156 mV/V with and without the ORI method, respectively. These results confirm that the symmetrical self-aligned source/drain region has significantly suppressed SCE by enhancing the vertical channel profile over the silicon pillar.

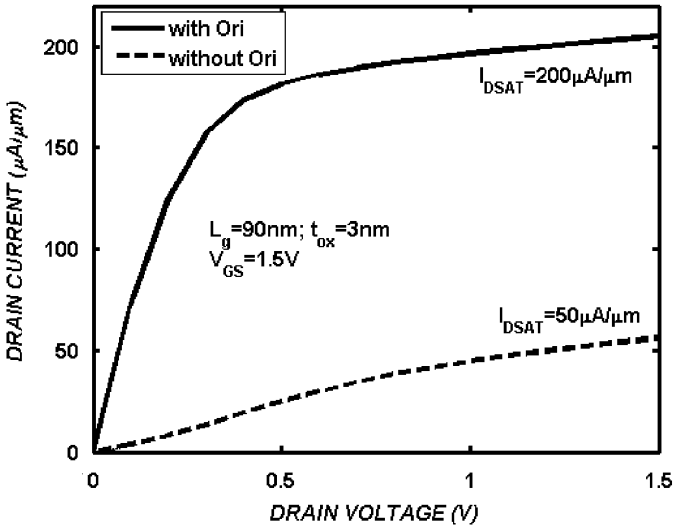

Fig. 5. Output characteristics of vertical double-gate MOSFET for both with and without the ORI method at $V_{GS} = 1.0$ V and $L_g = 90$ nm.

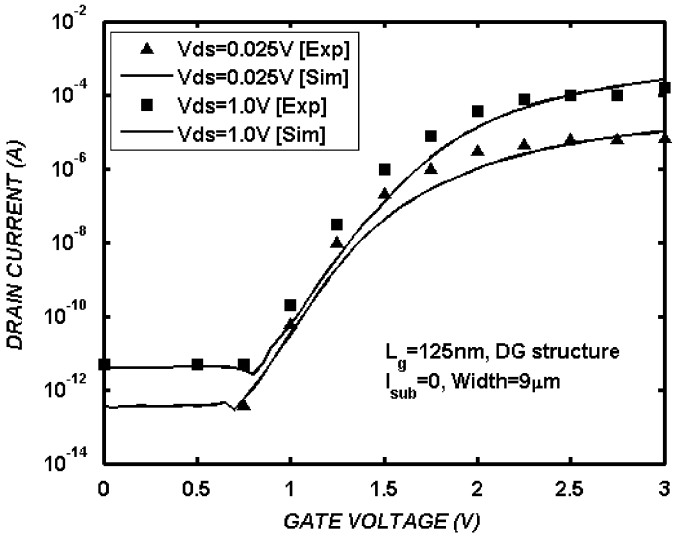

Fig. 6. Sub-threshold characteristics of vertical double-gate MOSFET for the fabricated device [7] and without the ORI method device at $V_{DS} = 25$ mV, 1.0 V and $L_g = 125$ nm.

Fig. 5 illustrates the comparison of output characteristics for 90 nm VDGM in ORI and without the ORI device at $V_{GS} = 1.5$ V. Due to the presence of non-self-aligned source/drain regions without using the ORI method, most of the injected electrons from the source are diffused into the substrate rather than swept away by the channel electric field. This increases the leakage current, thereby degrading the drain saturation current I_{DSAT} prominently as indicated in Fig. 5. $I_{DSAT} = 50\,\mu A/\mu m$ without the ORI method is very low. It enhances to $I_{DSAT} = 200\,\mu A/\mu m$ in an ORI device. In all respects, the ORI method presents a distinct advantage in improving the device performance.

In validating the simulation process, the simulated and experimental results of a device not using the ORI method are shown in Fig. 6. Excellent agreement between the simulated and experimental results on the 125 nm [7] device is indicative of the fact that the simulation process and the parameters used are valid. Fig. 6 also shows the high leakage current in the sub-threshold region and lower drive-on current in the saturation region. Therefore, the ORI method is distinctly advantageous.

6. Conclusion

Unique features of the vertical double-gate NMOSFET (VDGM) structure using the oblique rotating ion implantation (ORI) method is studied by means of device simulation and compared with fabricated device. With the ORI method, symmetrical self-aligned source/drain regions over the silicon pillar and sharp vertical channel profile are obtained. Sharp vertical channel profiles have increased the numbers of electrons in the channel injected from the source and decreased the channel length. These have improved the sub-threshold swing, drive-on current, leakage current, DIBL and drain saturation current significantly. The sub-threshold swing is shown to decline from 160 to 100 mV/dec and the threshold voltage V_T from 1.2 to 0.56 V, respectively. The drive-on current, I_{on}, has increased by a factor of 2 while DIBL reduced to 94 mV/V for $L_g = 90$ nm. The drain saturation current I_{DSAT} is shown to be sharply increased from 50 to 200 μA/μm. All of these results indicated that the SCE have been improved tremendously. The simulation process has been validated using the available experimental data. It is found that in many aspects the ORI method presents a distinct advantage in improving the device performance. Therefore, utilizing the ORI method in fabricating the unique structure of vertical MOSFET is prominently needed as scaling to the nanometer regime.

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